# Characterization of On-Chip Inductors

## Overview

- basic physics
- loss mechanisms
  - eddy currents in substrate / effect of ground shield
  - ohmic loss, skin and proximity effects in metal conductors
- optimization criteria
  - quality factor Q(f), f($Q_{max}$), self-resonant frequency $f_{sr}$,
- simulation examples with Ansoft HFSS (FEM-tool)

# Maxwell equations for time harmonic fields

Fields: $E = -j\omega A - \nabla\phi$

$B = \nabla \times A$

Assumptions:

- linear and isotropic metal and substrate conductors
- Coulomb gauge $\nabla \cdot A = 0$

$$\nabla^2 A = \mu\, [j\omega\sigma A \; - \; \omega^2 \varepsilon A + (\sigma + j\omega\varepsilon)\nabla\Phi \; - \; J\,]$$

term #: (1) (2) (3) (4)

(1) magnetically induced eddy currents in metal and substrate conductors

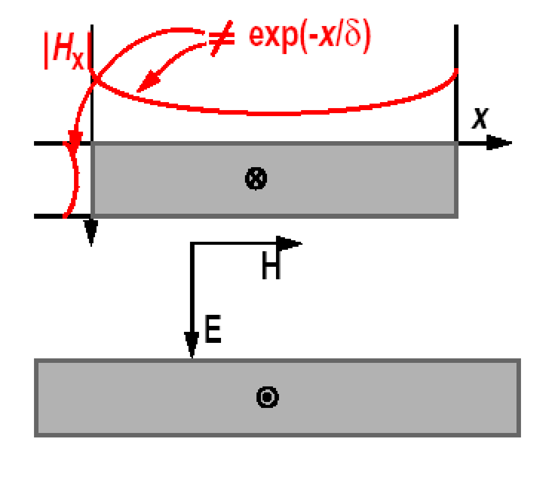
(2) dynamic radiation current (can be neglected here)

(3) electrically induced conductive and displacement currents

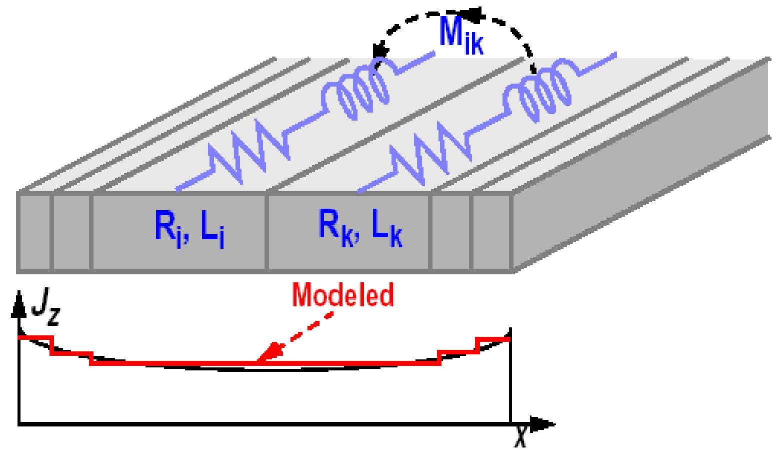
(4) impressed current in the metal conductors

# losses by currents (induced) in metal coil (I)

- ohmic loss (trivial)
- skin effect (inhomogenous current density due to magnetic field of single conductors, increases resistance)




Skin effect in rectangular conductor

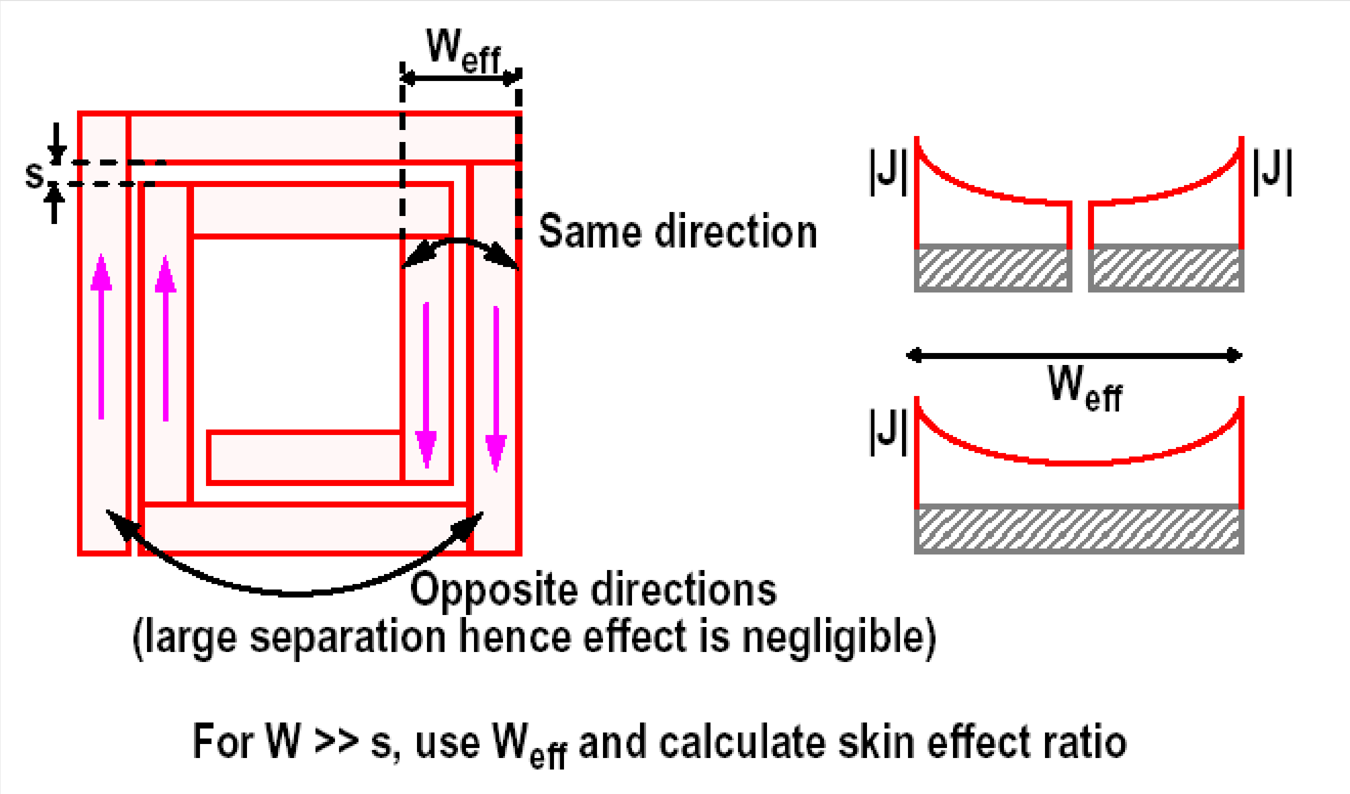



6 segments capture skin effect up to 20GHz.

from www.stanford.edu/~narya

# losses by currents (induced) in metal coil (II)

• proximity effect: similar to skin effect, but due to field from adjacent conductors)




from www.stanford.edu/~narya

# losses by currents induced in substrate

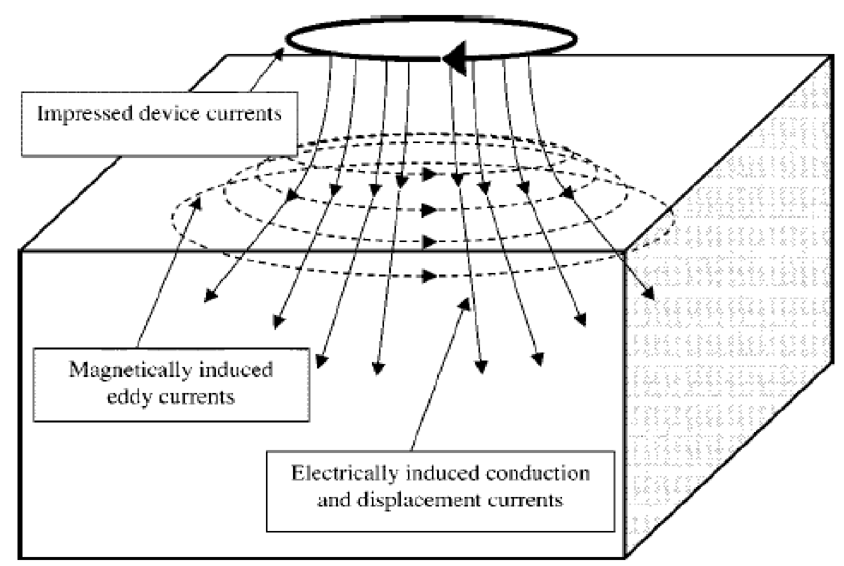


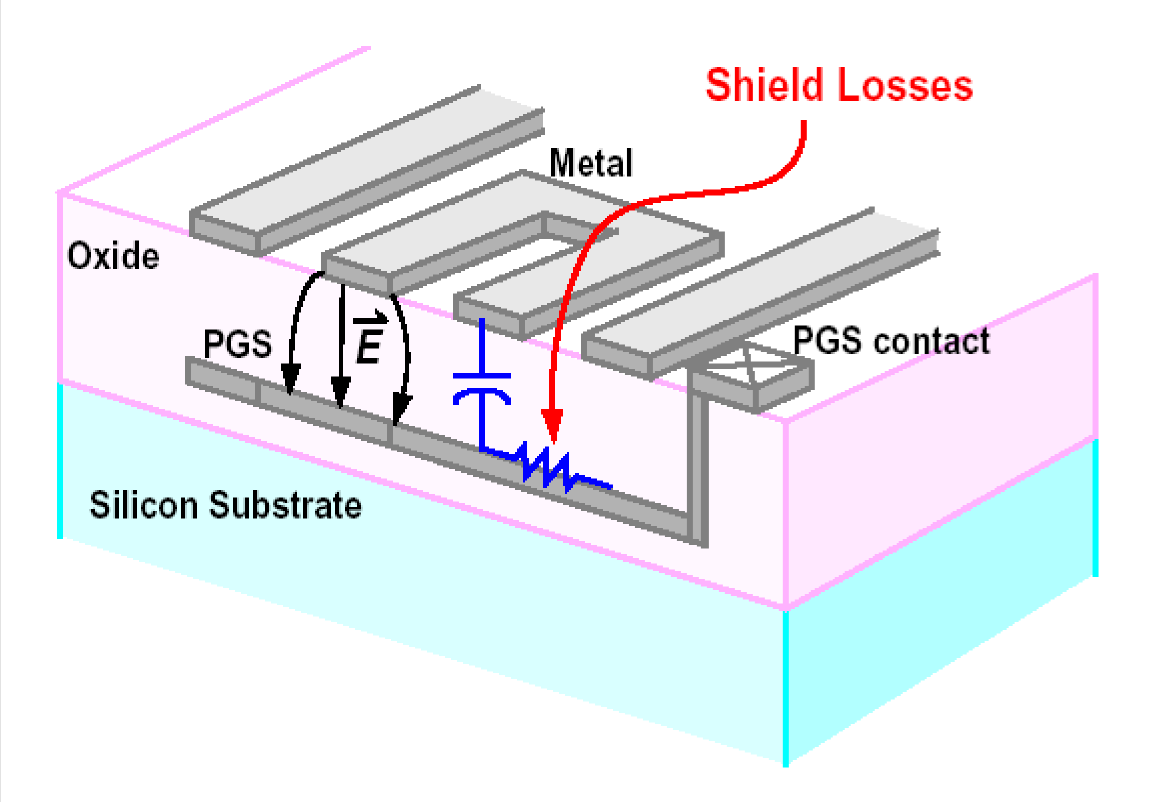

Fig. 2. Schematic representation of electrically and magnetically induced currents.

from Niknejad & Meyer, IEEE Trans. MTT 2001

magn. ind. currents : image currents, reduce inductance, cause ohmic loss

electr. ind. currents: through capacitive coupling to coil, also cause loss, and reduce self-resonance frequency (where Q = 0)

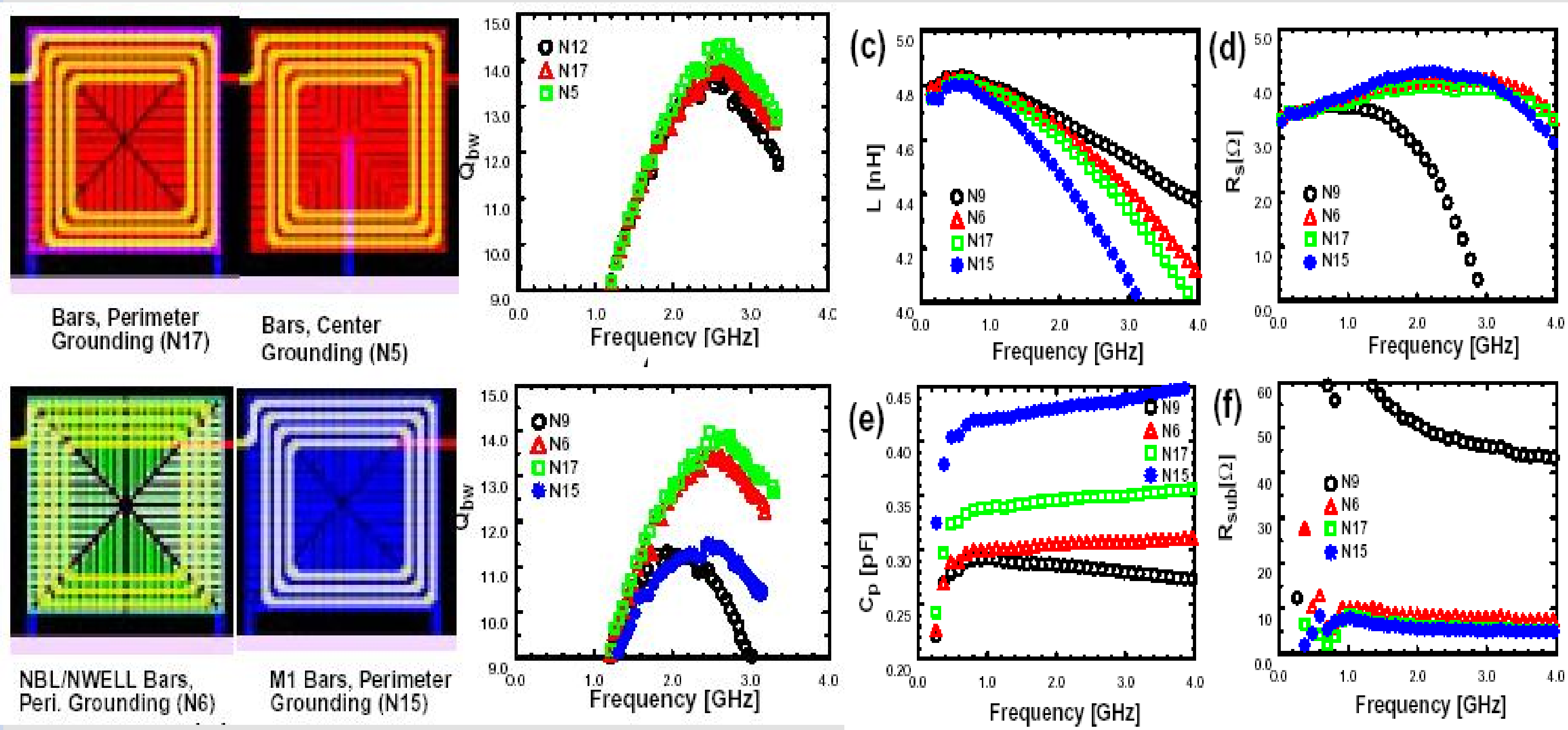
# effect of patterned ground shield




from www.stanford.edu/~narya

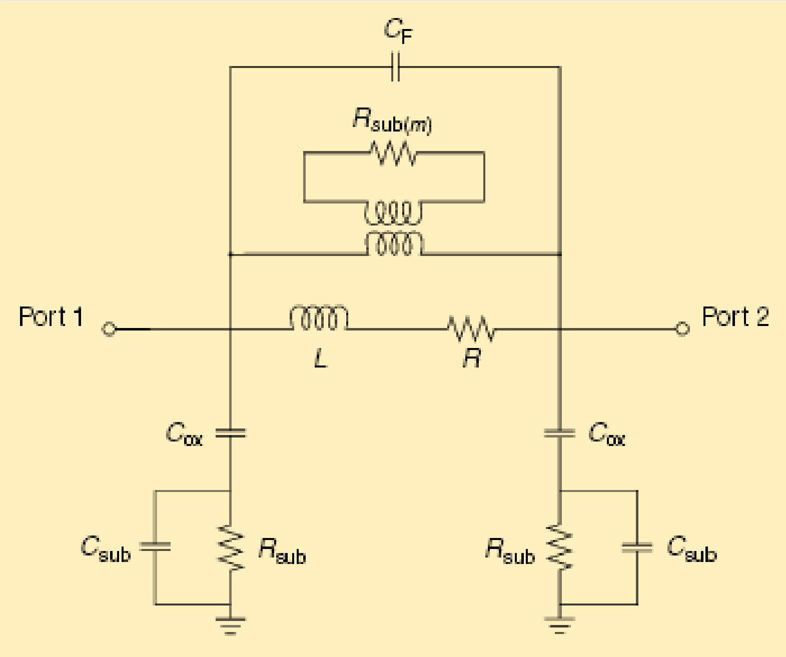
With optimized ground shield the substrate loss can be reduced substantially, thus increasing Q, with little change in inductance L and $f_{sr}$

# Patterned Ground Shields




**From: Seong-Mo Yim, Tong Chen, Kenneth K.O., Bipolar/BiCMOS Circuits & Techn. Meeting, 2000**

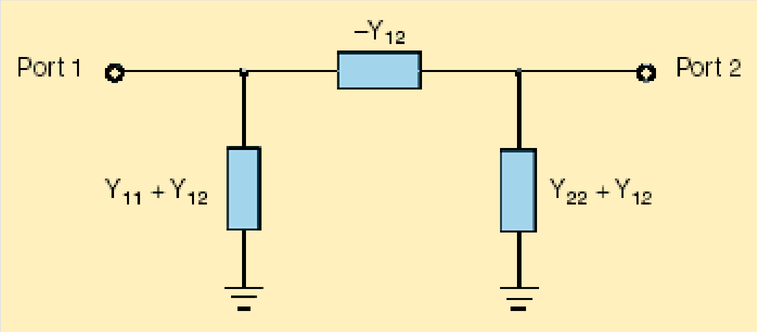
# spiral inductor circuit models




from Bunch, IEEE Microwave magazine June 2002

general spiral inductor lumped circuit model,

transformer models magnetically induced substrate eddy currents




$\pi$-equivalent circuit for two-port network

**For inductors used differentially (i.e. not one side grounded), S-parameters transformed to Y, then inductance L is defined as**

$$L = \mathrm{Im}\left(\frac{1/Y_{12}}{2\pi f}\right)$$

# Optimization criteria

## Quality factor Q(f)

measures ratio of maximum stored energy
to energy loss during one cycle

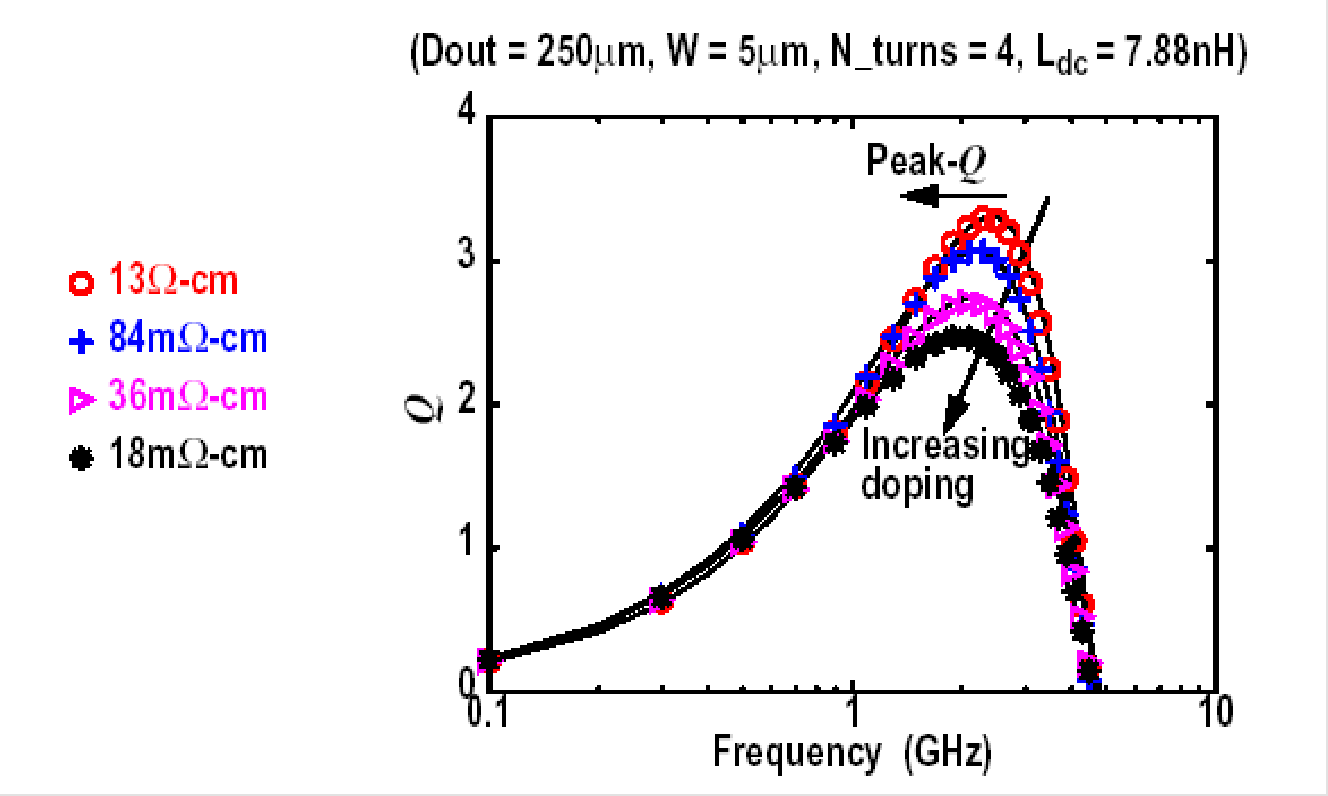
for low frequencies $Q \ \mu \ w \ L / R_{coil}$

at self-resonant frequency $f_{sr}$ : $Q = 0, \ (w_{sr})^2 \ \mu \ C / L$

for differentially used inductors:

$$Q = \frac{Im(1/Y_{12})}{Re(1/Y_{12})}$$

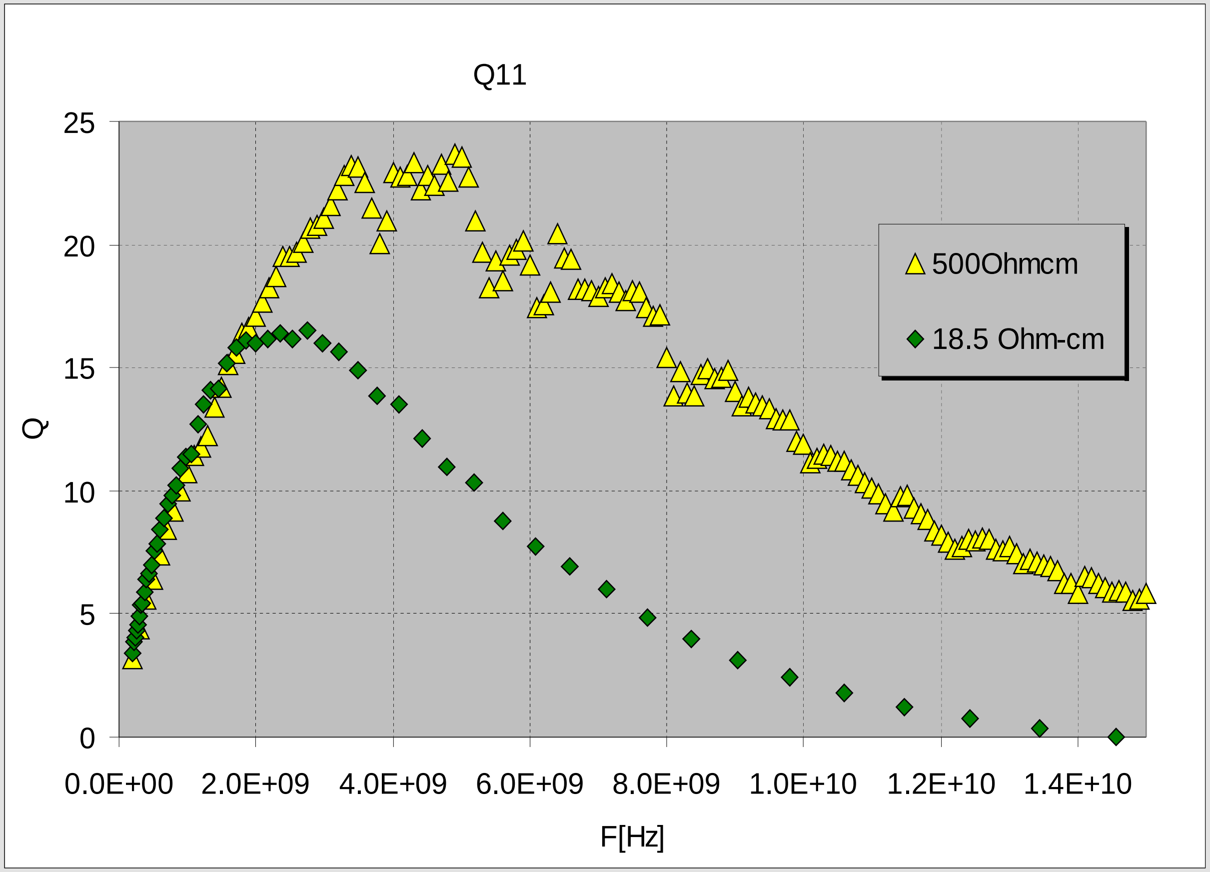
# effect of doping (substrate resistance) on Q(f)




from www.stanford.edu/~narya

**Lower doping: increases substrate resistance, reduces eddy currents and loss**

# Simulation with Ansoft / HFSS (I)



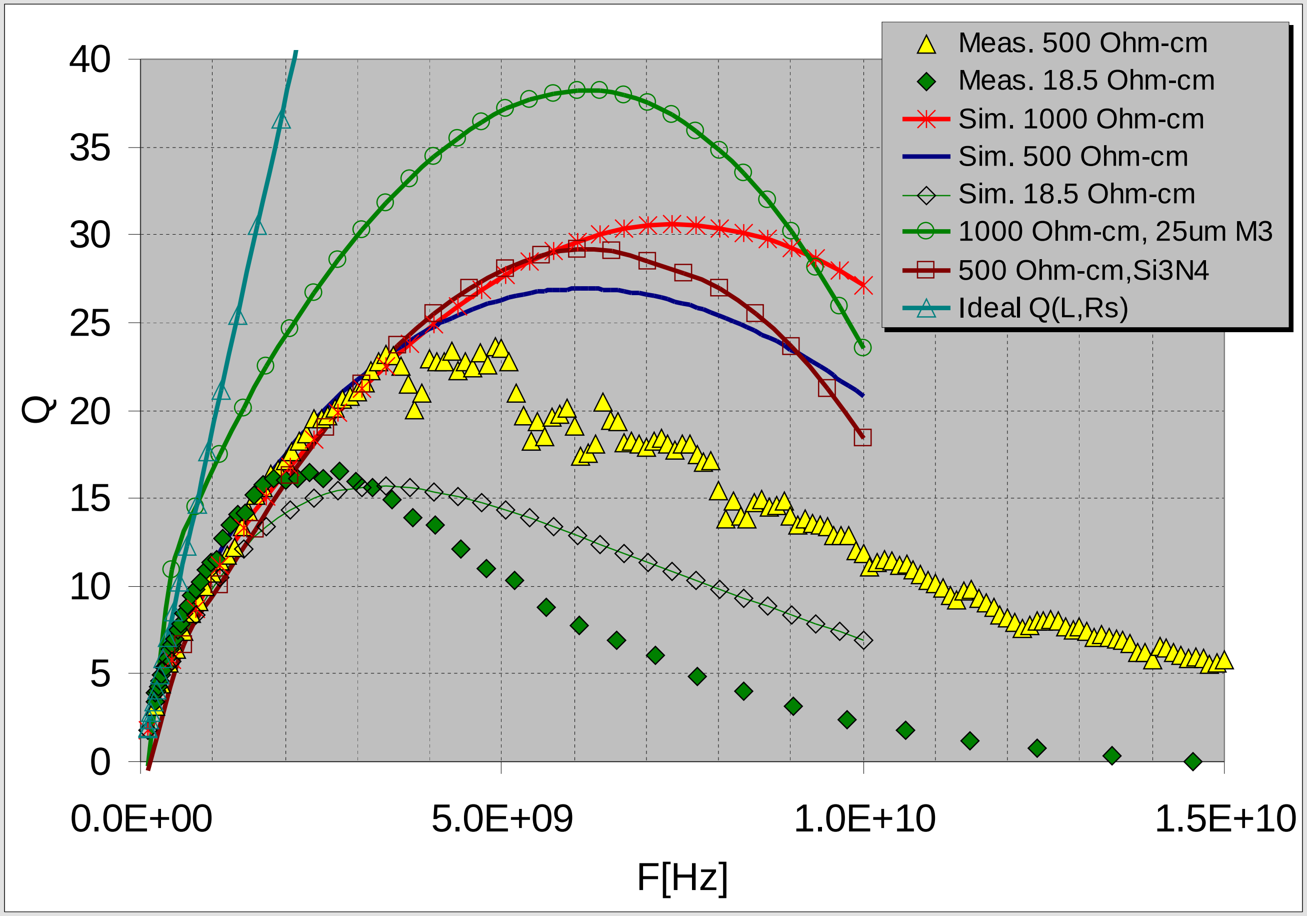

Remark:

Ansoft / **HFSS**
is a full 3D FEM
Maxwell eq. solver

Internal report from R. Strasser, IFX (CL TD SIM)

**Influence of substrate resistivity**

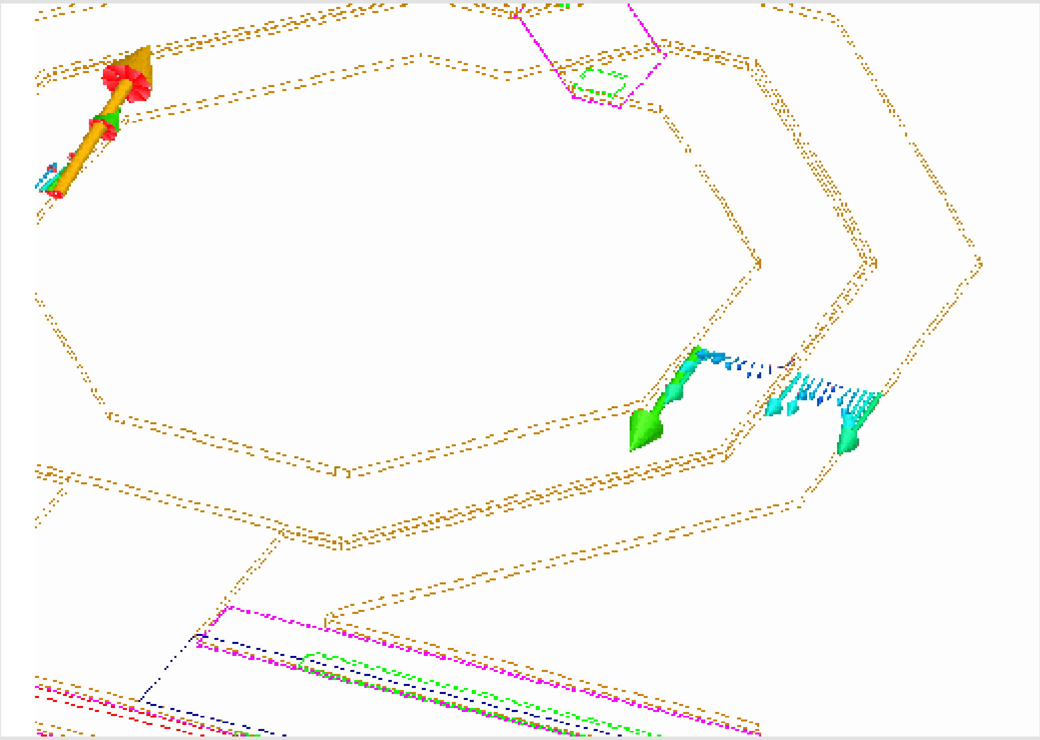
# Simulation with Ansoft / HFSS (II)




Internal report from R. Strasser, IFX (CL TD SIM)

**Comparison simulation / experiment**

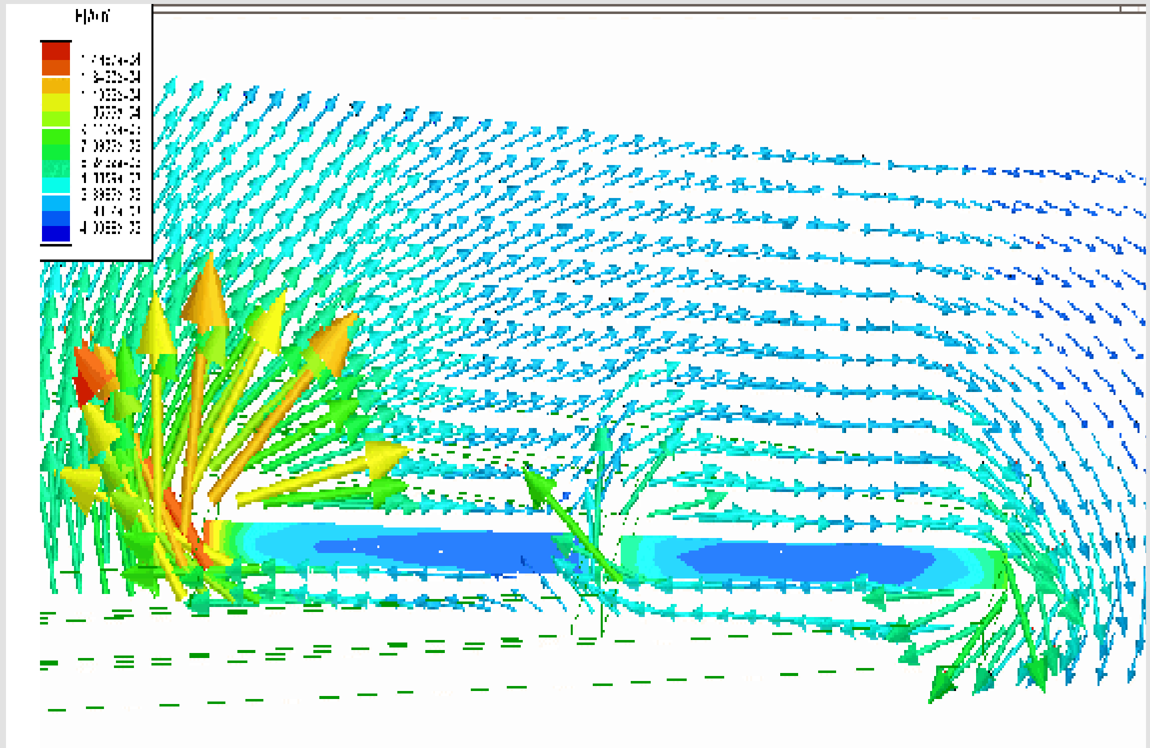
# Simulation with Ansoft / HFSS (III)



Internal report from R. Strasser, IFX (CL TD SIM)

**Current density at 2 GHz shows strong proximity effect**

# Simulation with Ansoft / HFSS (IV)



Internal report from R. Strasser, IFX (CL TD SIM)

**Relation between magnetic field and current density at 8 GHz.**
**Current crowding at cental hole (left) is strongest.**

# Final remarks

**some difficulties:**

- **FEM solver needs considerable CPU time** due to extremely small aspect ratio of typical on-chip inductors: width some 300 µm, metal thickness 1 to 3 µm (large mesh necessary)

- **simulation accuracy at high frequencies** for high resistance substrates not yet satisfactory (not well understood), there also deembedding of the measured devices is difficult.

**big advantage (!):**

- **simulation of on-chip inductors saves lots of time and money in development, good enough for optimization; only small final corrections are necessary**